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(54) Single-output dual-supply class D amplifier

(57) An amplifier (70) is formed by an astable multivibrator (2) having a signal output (15, 19) supplying a two-state output signal to a power stage (3), the output (35) of which presents an output voltage (V_o) switching between a first and second value; the output voltage presents a duty cycle varying with the input signal (V_{in}) of the multivibrator. The amplifier (70) is connected between a first and second supply line (V_{cc}, $-V_{cc}$) symmetrical with respect to ground (13) and subject to supply noise (ΔV), and comprises a current source (71) for generating the bias current of the astable multivibrator and supplying a current (I) switchable at each half cycle; the value of the current at each half cycle being proportional to the absolute value of the output voltage (V_o) of the amplifier, so as to vary the duty cycle of the amplifier in a manner correlated with the supply noise, so that the average output voltage value is zero.

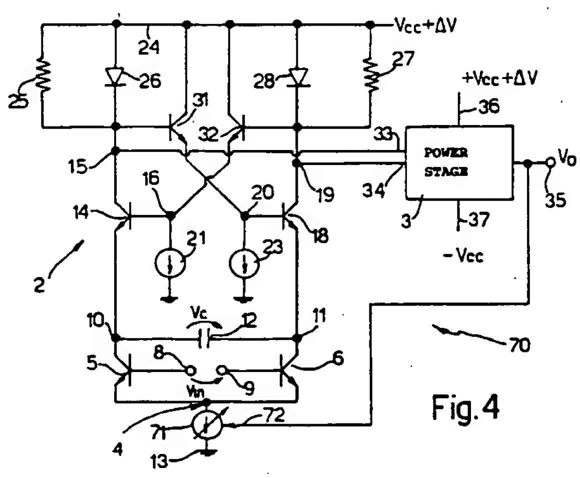

Fig.4

EP 0 753 934 A1

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Description

The present invention relates to a single-output dual-supply class D amplifier.

As is known (see H. R. Camenzind's article: "Modulated Pulse Audio Power Amplifiers for Integrated Circuits", IEEE Transactions on Audio and Electroacoustics, Vol. XV-14, N.3, September 1966), class D amplifiers are two-state or pulse-width modulation types, the output voltage of which is a rail-to-rail square wave varying between two reference voltages (in the case of dual supply, between the two supply voltages), with a duty cycle varying according to the input signal.

More specifically, and as shown in Figures 6 and 7 of the above article, a class D amplifier may be implemented by an astable multivibrator stage output-connected to a power stage, as shown in Figure 1, in which the amplifier is indicated as a whole by 1, the astable multivibrator stage by 2, and the power stage by 3.

Multivibrator stage 2 comprises a pair of input transistors 5, 6, in this case, two bipolar NPN transistors with their emitter terminals connected and forming a common node 4; a current I source 7 is provided between node 4 and a ground line (reference potential line) 13; the base terminals of transistors 5, 6 form the input terminals 8, 9 of amplifier 1, between which an input voltage V_{in} is supplied; the collector terminals of transistors 5, 6 define nodes 10, 11, between which is provided a capacitor 12; node 10 is connected to the emitter terminal of an NPN transistor 14, the collector terminal of which is connected to node 15, and the base terminal of which is connected to node 16; node 11 is connected to the emitter terminal of an NPN transistor 18, the collector terminal of which is connected to node 19, and the base terminal of which is connected to node 20; and bias current sources 21, 22 are provided respectively between nodes 16, 20 and ground 13.

Node 15 is connected to a positive supply line 24 at voltage V_{cc} via a resistor 25 and a diode 26 connected parallel to each other; similarly, node 19 is connected to supply line 24 via a resistor 27 and a diode 28 connected parallel to each other; an NPN transistor 31 has the collector terminal connected to supply line 24, the base terminal connected to node 15, and the emitter terminal connected to node 20; and a similar NPN transistor 32 has the collector terminal connected to supply line 24, the base terminal connected to node 19, and the emitter terminal connected to node 16.

Nodes 15 and 19 form the differential output of multivibrator stage 2, and are connected to respective inputs 33, 34 of the power stage, which presents an output node 35. In the example shown, power stage 3 is a dual-supply type, and therefore has a pair of inputs nodes 36, 37 supplied with two symmetrical supply voltages $+V_{cc}$ and $-V_{cc}$.

With a zero input signal V_{in}, the Figure 1 circuit operates as follows. If transistor 18 is on and transistor 14 off, the bias current supplied by source 7 flows through transistor 18 and resistor 27, which therefore directly biases and turns on diode 28; the voltage at node 19 equals $V_{cc} - V_{BE}$ (where V_{BE} is the voltage drop between the base and emitter of a turned-on NPN transistor, equal to the voltage drop across a diode, i.e. roughly 0.7 V); and the voltage at node 16 equals $V_{cc} - 2V_{BE}$. As transistor 14 is off, and disregarding the base current of transistor 31, the voltage at node 15 equals V_{cc}, the voltage at node 20 equals $V_{cc} - V_{BE}$, and the voltage at node 11 equals $V_{cc} - 2V_{BE}$. As input voltage V_{in} is zero, the current through transistor 18 (equal to current I of source 7) is divided equally between transistor 6 and capacitor 12, and charges capacitor 12 to gradually reduce the voltage at node 10 in relation to that at node 11. When the voltage at node 10 equals $V_{cc} - 3V_{BE}$, the voltage between the base and emitter of transistor 14 equals V_{BE} and transistor 14 is turned on; then, the collector current of transistor 14 via resistor 25 causes a voltage drop over diode 26 such as to turn it on. Therefore, the voltage at node 15 is brought to $V_{cc} - V_{BE}$; the voltage at node 20 is brought to $V_{cc} - 2V_{BE}$; transistor 18 is turned off (zero voltage drop between the base and emitter); diode 28 is turned off; the voltage at node 19 equals V_{cc}; the voltage at node 16 equals $V_{cc} - V_{BE}$; and the voltage at node 10 equals $V_{cc} - 2V_{BE}$. The bias current I generated by source 7 now flows from transistor 14, and is divided equally between capacitor 12 and transistor 5. More specifically, the current through capacitor 12 flows in the opposite direction to previously, and discharges the capacitor, the voltage V_c of which falls linearly from V_{BE} to $-V_{BE}$. As soon as voltage V_c reaches $-V_{BE}$, so that node 11 equals $V_{cc} - 3V_{BE}$, transistor 18 is turned on again to switch node 19 to $V_{cc} - V_{BE}$ and multivibrator stage 2 to the initial condition described.

At output nodes 15 and 19, multivibrator stage 2 therefore presents opposite phase voltages varying between two values, i.e. between V_{cc} and $V_{cc} - V_{BE}$, and which are supplied to power stage 3, a non-limiting embodiment of which is shown in Figure 2.

Power stage 3 in Figure 2 comprises a pair of P-channel MOS input transistors 40, 41, the gate terminals of which are connected respectively to nodes 33, 34; transistors 40, 41 are connected in a differential configuration, with the source terminals both connected to a current source 42, and the drain terminals connected to the drain terminals of respective N-channel MOS transistors 43, 44; transistors 43, 44 are diode-connected (shorted drain and gate terminals), and have the source terminals connected to a line 45 presenting negative supply voltage $-V_{cc}$ and connected to input terminal 37; transistors 43, 44 form current mirrors with transistors 47,48 and 49,50 respectively, which are all N-channel MOS transistors with the source terminal connected to line 45; the drain terminal of transistor 47 forms a node 51 connected to the emitter terminal of an NPN transistor 52, to the drain terminal of a P-channel transistor 53, and to the input of an inverter 54; transistor 52 has the collector terminal connected to a line 55,

and the base terminal connected to the output 35 of power stage 3, and to a first terminal of a bootstrap capacitor 56, the second terminal of which is connected to line 55; and transistor 53 forms a current mirror with a diode-connected P-channel transistor 57, the source terminal of which is connected to line 55, and the drain terminal of which is connected to the drain terminal of transistor 50.

Transistor 48 has the drain terminal connected to the drain terminal of a diode-connected P-channel transistor 59, the source terminal of which is connected to a node 60, and which forms a current mirror with a P-channel transistor 61, the source terminal of which is also connected to node 60, and the drain terminal of which is connected to the drain terminal of transistor 49 and to one input of an inverter 62.

Inverter 54 has two bias inputs connected respectively to line 55 and to the base terminal of transistor 52; and an output connected to the gate terminal of an N-channel power MOS transistor 64 forming the high-side output transistor. Inverter 62 has two bias inputs connected respectively to node 60 and to line 45; and an output connected to the gate terminal of an N-channel power MOS transistor 65 forming the low-side output transistor. The intermediate node between the source terminal of transistor 64 and the drain terminal of transistor 65 forms the output 35 of the power stage; the source terminal of transistor 65 is connected to line 45; and the drain terminal of transistor 64 is connected to supply voltage V_{cc}.

The circuit also comprises a regulated voltage source 68 between line 45 and node 60, and a diode 69 connected with its anode to node 60 and with its cathode to line 55.

Transistors 40, 41 form a differential stage and are therefore turned on alternately. More specifically, when the voltage at input 33 is at V_{cc} - V_{BE} and the voltage at node 34 is at V_{cc}, transistor 40 is on and transistor 41 off; in which case, transistor 40 drives the current mirror formed by transistors 43, 47, 48, which are on; node 51 is brought to a low voltage and the output of inverter 54 is high, so that transistor 64 is on and output voltage V_o is high (around V_{cc}); via transistor 48, transistors 59 and 61 are driven to supply a high voltage to the input of inverter 62; the output of inverter 62 is therefore low, and transistor 65 is off.

Conversely, when input 33 presents voltage V_{cc} and input 34 presents voltage V_{cc} - V_{BE}, transistor 40 is off and transistor 41 on; transistors 44, 49, 50 are therefore on; the input of inverter 62 is low, its output is high, and power transistor 65 is on to bring output 35 to $-V_{cc}$; transistor 50 drives the current mirror formed by transistors 53, 57, which are therefore on and bring node 51 to the high voltage on line 55; and transistor 64 is therefore off.

In the Figure 2 circuit, diode 69 and bootstrap capacitor 56 provide in known manner for charging capacitor 56 to the regulated voltage V_{REG} generated by source 68 when output node 35 is low and transistor 64 is off, and ensure correct biasing of high-side transistor 64 in the opposite phase when the gate terminal of transistor 64 must be driven at a voltage higher than supply voltage V_{cc} to ensure transistor 64 is turned on correctly and output 35 is latched to voltage V_{cc}.

Together, the Figure 1 and 2 circuits therefore supply the voltages shown in Figure 3, which shows a time plot of voltage V_c (long dotted line) and output voltage V_o (continuous line). In this case, the average output voltage value is zero.

Class D amplifiers such as the type described previously present a lower feedback rate than linear amplifiers, so that supply noise rejection (i.e. the logarithmic ratio between the output voltage and noise in the supply voltage) is low. That is to say, any noise in the supply is reproduced in a corresponding noise in the output; this problem is heavier in the case of single-output amplifiers than in bridge ones, in that, in a bridge amplifier, supply noise may be rejected as common-mode noise.

Since feedback fails to sufficiently reject supply noise, recourse must be made to other types of, e.g. feedforward, compensation. This type of compensation, however, is complicated in the case of dual-supply amplifiers of the type in question, which require noise rejection of both supplies.

For example, the presence of an asymmetric supply $V_{cc} + \Delta V_{cc}$, $-V_{cc}$, i.e. of noise in the high supply voltage, causes a variation in the output voltage V_o of the amplifier and in its average value. With reference to Figure 3, such an asymmetric supply would give rise to the output voltage V_o' shown by the dotted line and presenting an average value $V_{o,AVE} = V_{cc}/2$, i.e. a rejection of only -6 dB.

It is an object of the present invention to provide a class D amplifier of the type described, designed to overcome the aforementioned drawback.

According to the present invention, there is provided a single-output, dual-supply class D amplifier, as claimed in Claim 1.

A preferred, non-limiting embodiment of the present invention will be described by way of example with reference to the accompanying drawings, in which:

- Figure 1 shows a simplified circuit diagram of a known class D amplifier;
- Figure 2 shows a simplified circuit diagram of a portion of Figure 1;
- Figure 3 shows a time plot of a number of quantities in the Figure 1 diagram;
- Figure 4 shows an overall circuit diagram of the amplifier according to the present invention;
- Figure 5 shows a time plot of a number of quantities in the Figure 4 diagram;
- Figure 6 shows a detailed circuit diagram of part of the Figure 4 circuit.

Number 70 in Figure 4 indicates a class D amplifier presenting the same basic structure as in Figure 1, so that any parts common to both are indicated using the

same reference numbers with no further description.

According to one aspect of the present invention, the bias current source 71 between the emitters of transistors 5, 6 and ground line 13 is variable, and supplies an output current of a value related to the absolute value of output voltage V_o of amplifier 70, so as to vary its duty cycle. More specifically, the duty cycle is so modified as to produce an opposite variation in the average output voltage value to that produced by noise on one of the two supply lines, so that current source 71 presents a control input 72 connected to the output terminal 35 of amplifier 70.

The voltages obtainable with the Figure 4 circuit are shown in the Figure 5 graph, which assumes an asymmetric supply $+V_{cc} + \Delta V$, $-V_{cc}$, so that output voltage V_o switches between these two values. Current source 71 supplies an output current of $A(V_{cc} + \Delta V)$, where A is a multiplication constant, when output V_o is high, and a current of A^*V_{cc} when output V_o is low ($-V_{cc}$).

When this different value bias current is used in the two half cycles, capacitor 12 is supplied with a different current in each half cycle, and presents different charging and discharging speeds to give the triangular wave in Figure 5, the leading (higher current) edges of which are steeper than the trailing (lower current) edges. Consequently, the duty cycle of the circuit varies, and output voltage V_o presents half cycles of different length, and more specifically, a shorter half cycle T_1 when V_o is high, and a longer half cycle T_2 when V_o is low.

Thus, the average value of output voltage V_o is zero. In fact, since each half cycle is determined by the time in which the capacitor is charged or discharged, and its voltage varies by $2V_{BE}$:

$$T_1 = 2\,V_{BE}\,C/[A(V_{cc} + \Delta V)] \qquad (1)$$

$$T_2 = 2\,V_{BE}\,C/(A\,V_{cc}) \qquad (2)$$

where C is the capacitance of capacitor 12.

The average value $V_{o,AVE}$ of output voltage V_o equals:

$$V_{o,AVE} = [(V_{cc} + \Delta V)\,T_1 - V_{cc}\,T_2]/(T_1 + T_2) \quad (3)$$

Substituting (1) and (2) in (3):

$$V_{o,AVE} = 0$$

The circuit is therefore compensated for any asymmetrical variations in supply voltage.

One embodiment of variable current source 71 is shown in Figure 6 and described in detail below.

Figure 6 shows the Figure 4 node 4 common to the emitters of transistors 5, 6; node 4 is connected to the drain terminal of an N-channel MOS transistor 75, the source terminal of which is connected to node 76, and the gate terminal of which is connected to the gate terminal of a diode-connected (shorted drain and gate terminals) N-channel MOS transistor 77; node 76 is connected to the output node 35 of amplifier 70 via a resistor 78, and to the source terminal of a P-channel MOS transistor 79. Transistor 79 has its gate terminal connected to the gate terminal of another P-channel MOS transistor 80, and its drain terminal connected to the drain terminal of a diode-connected N-channel MOS transistor 81; transistor 81 presents its source terminal connected to a negative supply line 82 at $-V_{cc}$, and its gate terminal connected to the gate terminal of an N-channel MOS transistor 83 with which it forms a current mirror; transistor 83 has its source terminal connected to negative supply line 82, and its drain terminal connected to node 4.

Transistor 77 has its drain terminal connected, via a bias current source 85 of value I_b, to a positive supply line 86 at $V_{cc} + \Delta V$, and its source terminal connected to ground line 13; and diode-connected transistor 80 has its source terminal connected to ground line 13, and its drain terminal connected to negative supply line 82 via a constant current source 87 also of value I_b.

Variable current source 71 operates as follows. Since transistors 77 and 75 present substantially the same gate-source voltage drop (as regards the operating conditions of the circuit, the two voltage drops differ by only a few hundred mV, which is negligible in relation to the supply voltages of devices of this type - normally a few tens of volts or even higher), the source terminal of transistor 75 (node 76) may be assumed to be at the same potential as the source terminal of transistor 77 (ground), and the terminals of resistor 78 to present a voltage drop equal to output voltage V_o of amplifier 70.

Given an initial voltage V_o of $V_{cc} + \Delta V$, so that voltage $V_{cc} + \Delta V$ is present between node 35 and node 76, a current $I_1 = (V_{cc} + \Delta V)/R$ from node 35 flows through resistor 78 of resistance R, and transistors 75, 79 operate more or less as a differential circuit. More specifically, when output voltage V_o is positive, the voltage at node 76 also tends to be slightly positive, so that transistor 79 is on and transistor 75 is off; and current I_1 flows through transistors 79 and 81, is mirrored in transistor 83, and is drawn by node 4. In this phase, current I therefore equals I_1 and enters the Figure 6 circuit.

When voltage V_o switches to $-V_{cc}$, voltage V_{cc} is present between node 76 and node 35, so that a current $I_2 = V_{cc}/R$ opposite in direction to I_1 (directed towards node 35) flows through resistor 78. In this phase, the voltage at node 76 tends to be slightly negative, so that transistor 75 is now on and transistor 79 off; and current I_2 flows through transistor 75 and is drawn by node 4. In this phase, current I therefore again enters the Figure 6 circuit, but equals I_2.

In other words, source 71 in Figure 6 generates a current I_1, I_2 proportional to the absolute value of output voltage V_o of amplifier 70 in the half cycle considered, wherein proportion constant A of equations (1)-(3) in this case equals 1/R where R is the resistance of resistor 78.

Clearly, changes may be made to the amplifier as described and illustrated herein without, however,

departing from the scope of the present invention. In particular, it should be stressed that the Figure 6 circuit is only one of many possible implementations of the variable current source.

Claims

1. A single-output, dual-supply class D amplifier (70) comprising an astable multivibrator stage (1) defining at least one signal input (8, 9) supplied with an input signal (V_{in}), and a signal output (15, 19) supplying a two-state output signal; said signal output being connected to a power stage (3) defining a power output (35) of said amplifier and generating an output voltage (V_o) switching between a first and a second value defining a duty cycle of a value correlated with said input signal; said amplifier (70) being connected to a first and second supply line (24, 45) at symmetrical supply voltages in relation to a reference potential line (13) and subject to supply noise; characterized in that it comprises means (71) for varying said duty cycle in a manner correlated with said supply noise.

2. An amplifier as claimed in Claim 1, wherein said astable multivibrator stage comprises a first (5, 14, 25, 26) and second (6, 18, 27, 28) branch substantially in parallel; a current source (71) connected to said first and second branch and generating a bias current (I); and a capacitor (12) located between said first and second branch, and flown by at least part of said bias current alternately in opposite directions, said capacitor determining a sequence of charging and discharging steps and an output signal switching step; characterized in that said current source (71) is a switchable current source for generating a current of a value correlated with the instantaneous absolute value of said output voltage (V_o).

3. An amplifier as claimed in Claim 2, characterized in that said switchable current source (71) presents a control input (72) connected to said power output (35) of said amplifier (70).

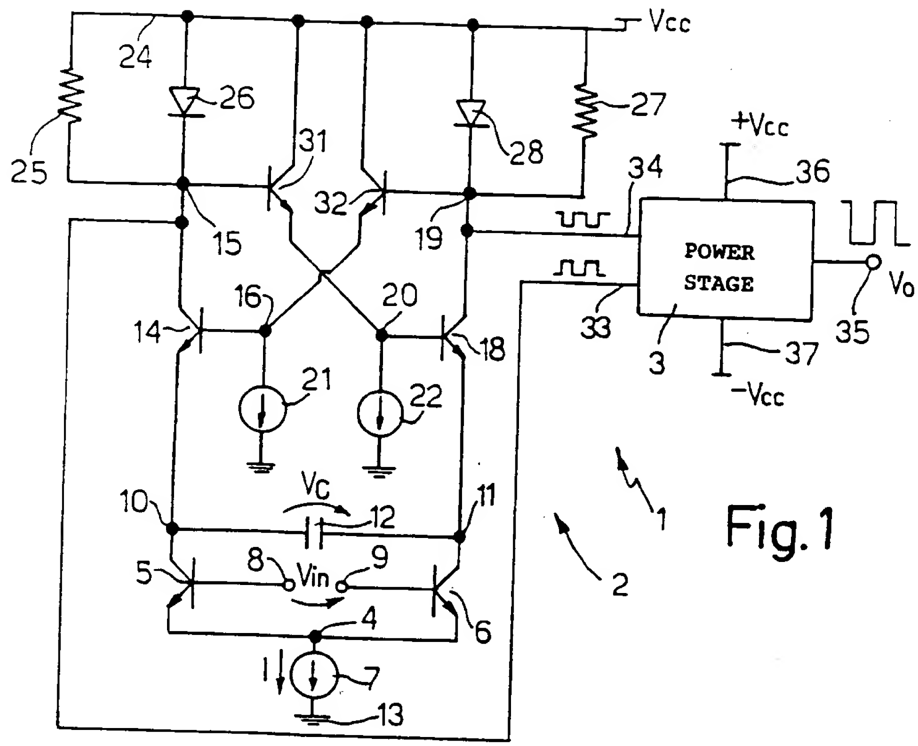
4. An amplifier as claimed in Claim 3, characterized in that said switchable current source (71) comprises a differential element (75, 79) having an input (76) connected to said power output (35) via a resistive element (78), a first and second terminal connected to a common node (4) of said first and second branch (5, 14, 25, 26, 6, 18, 27, 28), and a third and fourth terminal connected to first and second bias means (77, 80).

5. An amplifier as claimed in Claim 4, characterized in that said differential element comprises a first (75) and second (79) transistor of opposite types having a first and second terminal and a control terminal; said first terminal of said first transistor (75) being connected to said common node (4) of said first and second branch (5, 14, 25, 26, 6, 18, 27, 28); said second terminal of said first transistor (75) being connected to said power output (35); said control terminal of said first transistor being connected to said first bias means (77); said first terminal of said second transistor (79) being connected to said common node (4) of said first and second branch (5, 14, 25, 26, 6, 18, 27, 28); said second terminal of said second transistor (79) being connected to said second terminal of said first transistor; and said control terminal of said second transistor being connected to said second bias means (80).

6. An amplifier as claimed in Claim 5, characterized in that said first terminal of said second transistor (79) is connected to said common node (4) via a current mirror circuit (81, 83).

7. An amplifier as claimed in Claim 5 or 6, characterized in that said first bias means comprise a third transistor (77), and said second bias means comprise a fourth transistor (80); said third and fourth transistor being of opposite types, being diode-connected, and having a first and second terminal and a control terminal; said first terminal of said third transistor (77) being connected to a first current source (85); said second terminal of said third transistor (77) being connected to said reference potential line (13); said control terminal of said third transistor being connected to said control terminal of said first transistor (75); said first terminal of said fourth transistor (80) being connected to a second current source (87); said second terminal of said fourth transistor (80) being connected to said reference potential line (13); and said control terminal of said fourth transistor (80) being connected to said control terminal of said second transistor (79).

8. An amplifier as claimed in Claim 7, characterized in that said first and third transistor (75, 77) are N-channel MOS transistors, and said second and fourth transistor (79, 80) are P-channel MOS transistors.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19
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+Vcc
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POWER
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Fig.1

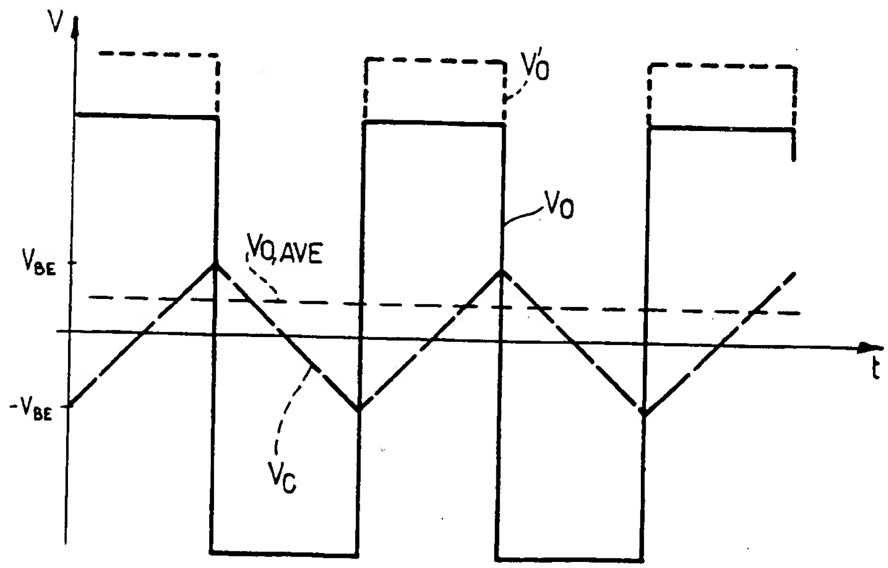
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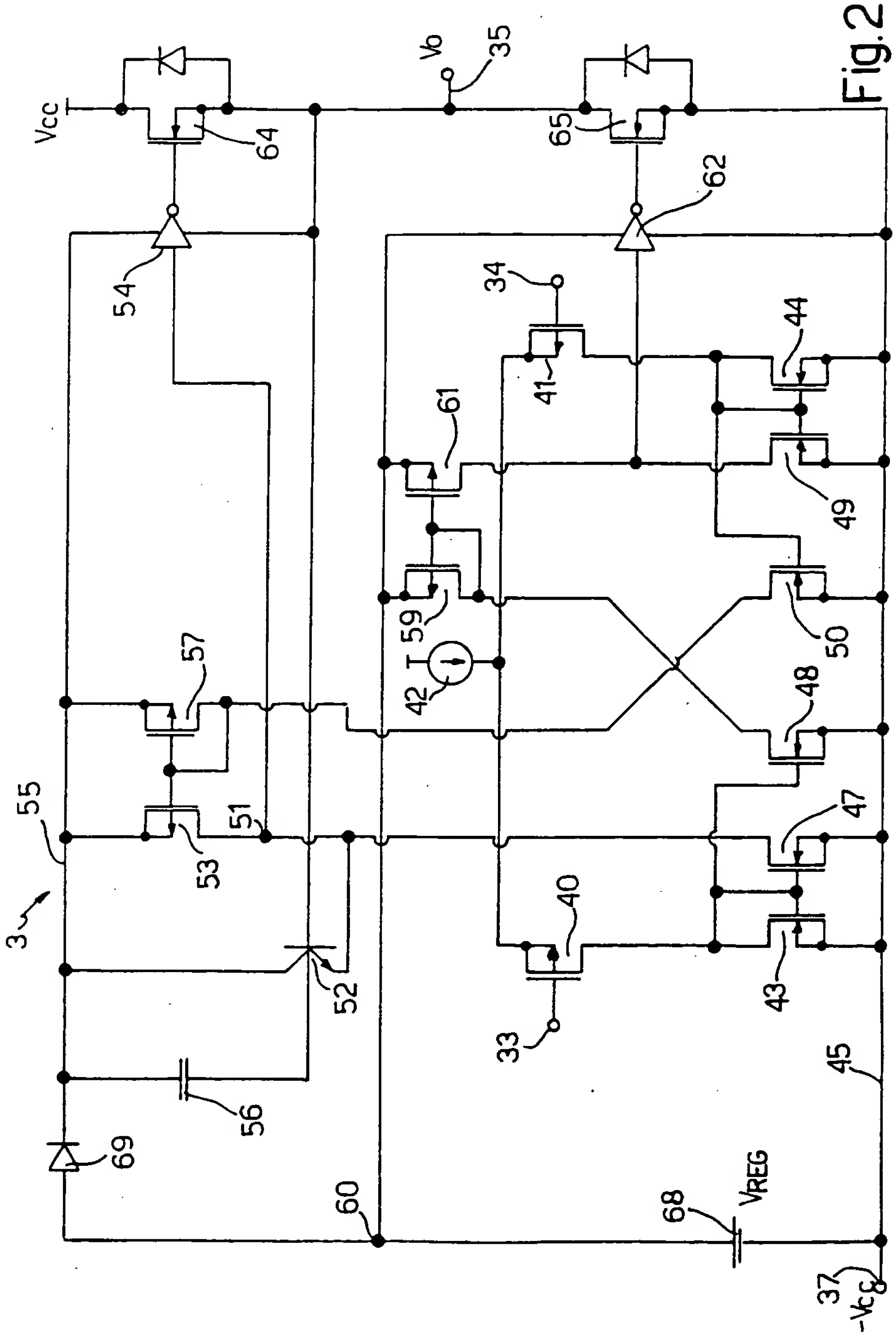
Fig.3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VREG
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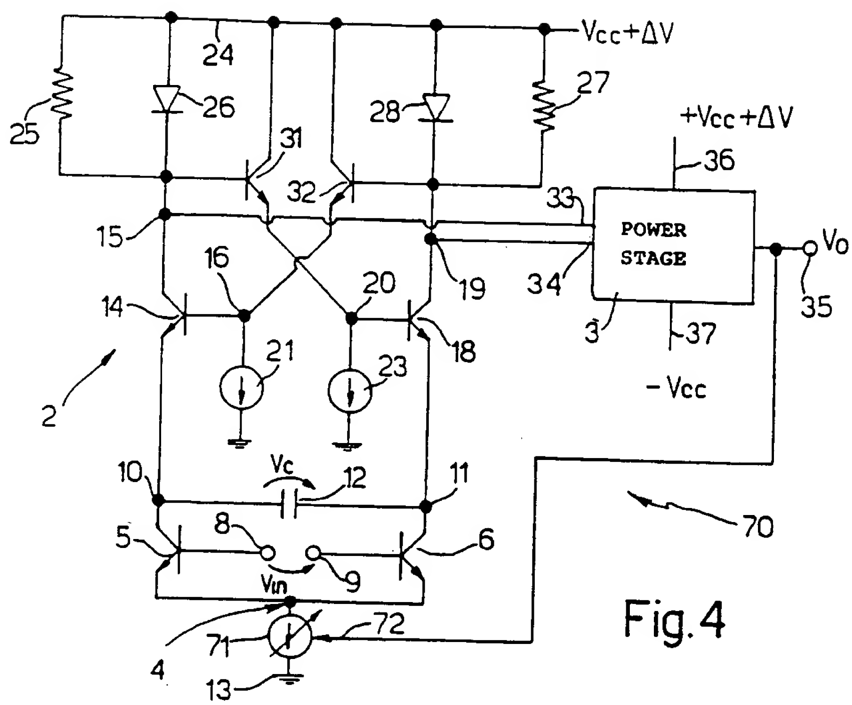
-Vcc

Fig.2


Vcc+ΔV
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+Vcc+ΔV
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14
18
3
37
21
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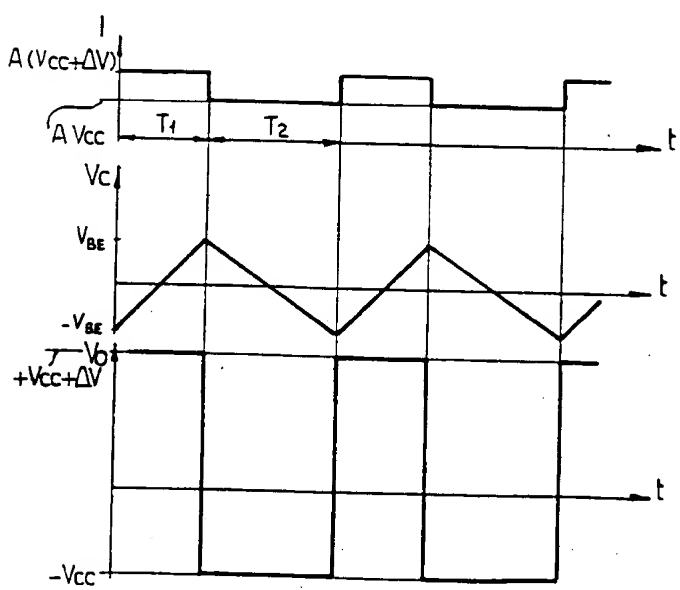
72
71
4
13

Fig.4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VBE
-VBE
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Vo
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-Vcc

Fig.5

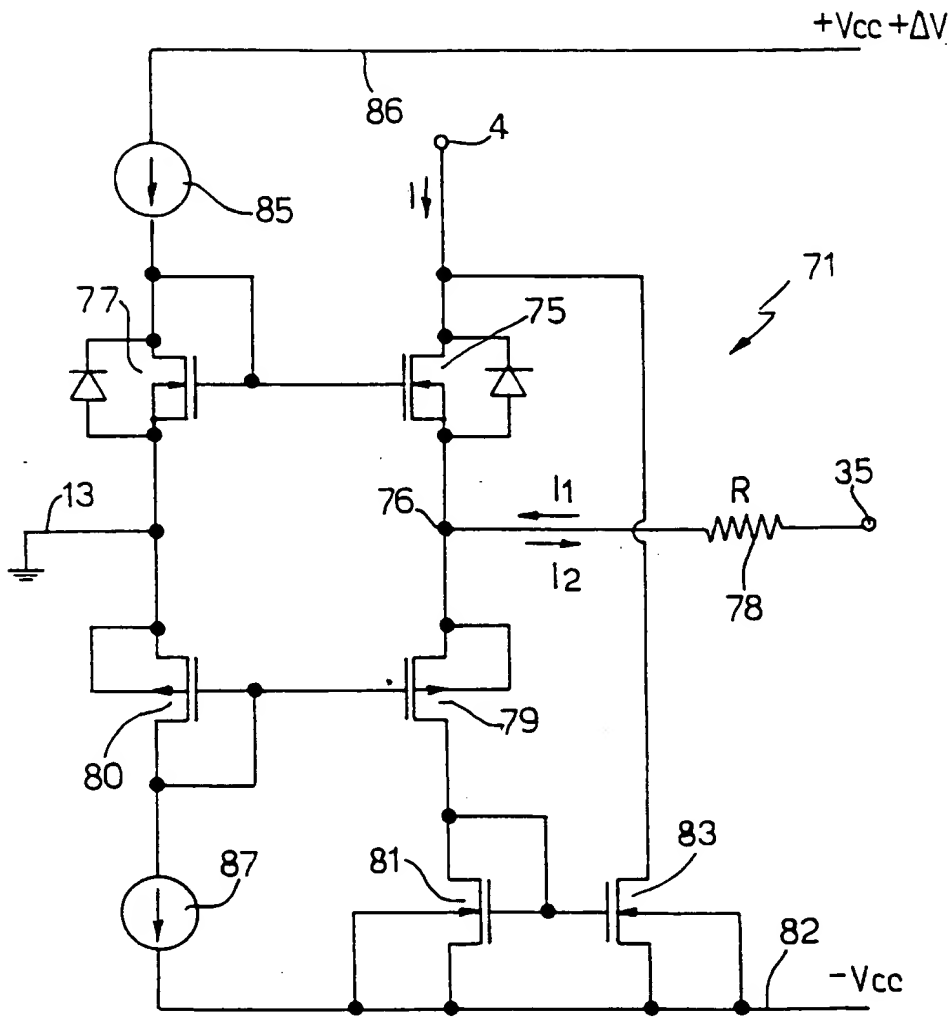

Fig.6

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EUROPEAN SEARCH REPORT

Application Number
EP 95 83 0301

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y A	EP-A-0 503 571 (MATSUSHITA ELECTRIC INDUSTRIAL CO) * the whole document *	1-5 6,7	H03F3/00 H03F3/217 H03K3/282
Y	US-A-5 289 502 (S. KAWASAKI) * the whole document *	1-5	
Y A	US-A-5 412 349 (YOUNG I. ET AL) * abstract; figures 2A ,2B ,3B *	1-5 8	
A	EP-A-0 277 682 (PHILIPS PATENTVERWALTUNG GMBH) * the whole document *	1-5	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H03F
H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	1 December 1995	Tyberghien, G

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